Amendments to the Specification:

Please replace paragraph **19** with the following amended paragraph:

[0019] A planarized copper layer 113 is overlying the insulating layer. The planarized copper layer includes a surface region at a height at about the substantially planar surface region and/or a height above or slightly below depending upon the specific embodiment. The planarized copper layer can be formed by deposition/plating and planarization techniques, which will be described in more detail below. As shown, a second electrode is formed from a portion of the planarized copper layer to define the capacitor structure. An interconnect structure 108 is also shown in Figure 1. Certain features of the present structure can be found in specifically below.

Please replace paragraph **44** with the following amended paragraph:

[0044] Referring to Figure 3, the method forms a mask 301 on a surface overlying exposed dielectric material. The mask can be a photolithographic material, which is developed and patterned. The region between the two damascene structures is exposed and patterned. Here, the method performs a plasma etch process to remove first portion of the exposed dielectric material. The method then selectively etches via wet etch to selectively remove second portion of the exposed dielectric material to the barrier material, as illustrated by Figure 4. The method then forms a capacitor dielectric 111 within opening defined by the above etching processes. The capacitor dielectric can be any suitable material, e.g., silicon nitride, oxide, any combination of these. The capacitor dielectric is provided by chemical vapor deposition. The method forms a barrier 501 (e.g., tantalum and tantalum nitride) within the opening overlying the capacitor dielectric. Referring to Figure 5, the method fills in the opening with copper material 503. The copper material is often planted using well known techniques. Next, the copper material is planarized using chemical mechanical polishing. The remaining portion of region 503 defines a second capacitor plate. Depending upon the embodiment, there can be other steps as desired. Depending upon the application, certain steps may be combined or even separated. Certain steps may be performed in other order or sequence also depending upon the embodiment. Other steps may be added or steps may be omitted depending upon the embodiment.